3.5 Timing and RF Distribution

3.5.1 Overview

The sequence of events in one cycle is as follows:
The Booster septum Si is triggered.
The Linac klystron modulator is triggered, and the Linac RF is established.
The Booster kicker Ki is triggered.
The Linac cannon is turned on and off very precisely to fill one or several RF buckets in the booster.
Over the next 200msec (or longer), all the Booster magnet currents and the Booster RF are ramped up;
The Booster extraction septum Se and the Storage Ring injection septum S12 are triggered.
The Storage Ring kickers K1, K2, K3 and K4 are triggered
The Booster Extraction kickers Ke1 and Ke2 are triggered

Over the next 100msec, all the Booster magnet currents and RF are ramped down, and all the pulsed power supplies are recharged for the next pulse.

If a Resonant Supply would be used to ramp the Booster magnets up and down, the moment when the magnetic field is correct for injection or extraction must be measured; the measurement pulse is applied asynchronously as an input (eg "Gauss Clock") to the Bunch Clock circuit. The moment when the timing pulse is sent to the equipment is quantised. However, there is an unknown delay or jitter between zero and N times the RF period in this signal. Further, there is only a narrow "window of opportunity" of a few microseconds when the Booster magnet currents give the correct particle energy.

Fortunately, the SLS Booster is not driven by a Resonant Supply, but by a Programmed Ramp Supply. The moment when the timing pulses are send to the equipment is still quantised. However, the quantisation step size becomes irrelevant; the whole machine has the same quantisation, so there is no synchronising jitter. The Booster power supplies are programmed to increase in steps of one Booster rotation period, and can readily be programmed to have a "window of opportunity" of many microseconds when the particle energy is exactly constant.

A overview of equipment placement is shown in Fig.f291_a.

3.5.2 RF Source and Phase Noise

The exact source frequency would be adjusted to compensate for a change in mean length of the electron beam path in the Storage Ring. As an estimate from other accelerators, a change of 3mm in 288m, or 10ppm would be typical; thus the RF would be 500MHz +/-10ppm, or +/-5kHz. The RF source frequency would be updated a few Hertz every hour or so to account for thermal drift. Normally, klystron transmitters are tolerant of phase jumps that may occur when the frequency is being updated.

A comparison was made of published phase noise characteristics of common commercial signal sources, and the results are shown in Fig.f351_a. Initial calculation and experience in other accelerators shows that these phase noise levels are adequate for use in the SLS.



Fig. 3.5.1 Typical phase noise of signal sources.

3.5.3 VME Timing Requirements

Data acquisition at each of the dozen Control Stations needs to be synchronised. The minimum requirement is to provide synchronising pulses for the BPM acquisition. The bandwidth of the BPM electronics is typically 2kHz, with a maximum of 10kHz, so the requirement is to synchronise these acquisitions across the machine to $<0.1 \times 1/10$ kHz, or <+/-5µsec precision.

A few of the VMEs are also controlling the Injection/Extraction supplies and the Booster power supplies. The timing precision should be <+/-20nsec for these supplies.

There are future options for time-resolved experiments, and for turn-by-turn BPM acquisition which (in the limit) demands accuracy to below half of one RF period, or <+/-**1nsec**. A further consideration is that the exact location of the BPM pickups and the exact BPM cable lengths are not known. The local timing would require some sort of fine adjustment with a resolution of 1nsec. In principle, this timing could be derived directly from the circulating beam, since small phase changes from synchrotron oscillation would not affect the measured result.

Finally, for time study of the electron beam itself, a source is required with short-term phase stability below $\pm -0.18^{\circ}$. Although undesirable, slow thermal drift of phase over a period of tens of minutes could be tolerated for this.

3.5.4 Signal Transmission

The initial development was performed with a 150m, 10-way, commercial fibre optic cable (Ref.0). The delay variation was +6.7 (\pm 0.5)ps/°C for the complete 150m length of cable, plus +7.8(\pm 1)ps/°C for the electronics. The highly linear temperature coefficient makes this a good candidate for electronic thermal compensation. The jitter was <70psec RMS. The weakest part of the system was the connectors, since a large attenuation change (eg dirt or incomplete insertion) could result in a time change in the order of a hundreds of picoseconds; however this can be circumvented by splicing the fibres, or gluing the connectors after installation.

The cable lengths from the control room to the VME racks are estimated to be 33m - 130m. Since the fibre optic cables are not bulky, the spare cable can be coiled up in a 19" rack. Preterminated equal lengths of 130m for all the VMEs would be purchased and tested before installation. In this way, the differential timing drift between VMEs can be reduced, although the absolute drift with respect to the RF remains. These cables are to be used for control of the VMEs by the SLS Control Group.

A limitation of cheap data transmitters / receivers for fibre optic would be modest S/N. This problem can be reduced for narrow-band signals by filtering. However, broadband signals with a bandwidth above 100MHz would operate with S/N amplitude ratio of around 200.

To resolve the future option for good short-term phase stability, the choice was made to include, in parallel with the fibre optic cable, a standard 1/2" copper coaxial cable. This cable carries a 500MHz signal which can be used to re-synchronise the data at the receiving end with a jitter (with respect to a distant observer) in the picosecond region.

As a general rule, the cable lengths are short for the SLS, so it is the electronics for sending timing and RF signals that dominate the temperature drift. To minimise this, a novel feature may be used. Each electronic module is equipped with a heater / fan controlled by a temperature sensor. By this, the electronics can be stabilised to 32° +/- 2° C with little effort.

3.5.5 RF Distribution

There are only four signals which demand both short-term and long-term stability, the RF for the Linac, the Booster, the Storage Ring and the pulse signal to the Linac gun. The requirement is set by choosing a time error equal to the design bunch length at the moment of beam transfer between machines. The booster bunch length is 12mm, and the minimum Storage Ring bunch length is 3mm.

Thus RF time/phase between the linac cannon, linac cavities and booster cavities must be synchronised with a stability of <+/-6mm, or +/-20psec, or $+/-3.5^{\circ}$ at 500MHz. The RF time/phase between the booster cavities and storage ring cavities must be synchronised with a stability of <+/-1.5mm, or +/-5psec, or $+/-0.9^{\circ}$ at 500MHz.

A standard coaxial cable used in other accelerators would have a typical phase change of 10ppm/°C. A temperature change of 10°C over 50m gives an RF phase change of 4.48° (equivalent to 24.9ps). A differential phase drift with temperature in connecting cables is partially compensated by having equal cable lengths, as shown in Fig. f355_a. In addition,

the frequency is expected to be adjusted (Section 3.5.2) by +/-10ppm. The total phase change through a cable is increasing with length, and at 50m, a 10ppm frequency change gives a 0.4° phase change.



As the average temperature changes, so the electrical length of all the cables change at about the same rate. In this way, phase stability of $<+/-1^{\circ}$ between the receiving ends is possible. Development work has started on electronics which can send and receive 500MHz (without reflections) on these cables, and with a stability considerably better than $<+/-1^{\circ}$. As part of this equipment, a equal-length return cables will be installed to permit continuous monitoring of the go-and-return phase, and if necessary the equipment can be upgraded to include active phase compensation.

3.5.6 Machine Timing Receiver

The following outlines the interface that will be seen by the Control Group and by experimentalists at each of the VMEs. Referring to Fig.3.5.3, the Machine Timing Receiver is a 1U, 19" electronics module with a row of BNC connectors on the rear panel. These connectors output AC coupled pulses of >0.9V amplitude into 50 Ω . The pulses all have typical rise / fall times of 400ps, and have <100psec skew between themselves. The pulses are all positive edge, and are all multiples of 60nsec long. The signals are:

Bper	pulse per Booster period
SRper	pulse per Storage Ring period
Binj	pulse a few microseconds before the Booster septum Si is triggered
SRinj	pulse a few microseconds before the Booster septum Se is triggered
Cycle	pulse at the start of a Booster cycle
DAQ	pulse at a programmed delay before SRinj, eg 15.36msec
Spare	

Internal to the Machine Timing Receiver there are another nine timing channels that could be used for future upgrades.



Fig.f356 a: Front and rear panels of the Machine Timing Receiver.

On the front panel, there are two indicators "Booster Inject" and "Storage Ring Inject" connected to the BRinj and SRinj signals. These LEDs will flash continually while the unit is functioning correctly. If the incoming data has even one bit error, the "Error" LED will blink on, but the "Latched Error" LED will turn on and stay on; the Latched Error LED can be turned off by pressing the RESET button.

3.5.7 Overview of Synchrotron Timing

There are two basic approaches to the problem of synchronising the transfer between buckets of two accelerator rings: either the time of transfer is fixed, and the RF is phase adjusted to advance or retard the rings to align them; or the RF phase of the two rings is fixed, and the transfer takes place after waiting for a programmed time delay. Both techniques have been used at other accelerators;

Phase adjustment offers the following possibilities:

- phase / frequency modulation of the source (eg diagnostics);
- detailed study of the injection / extraction / energy ramping
- optimisation the Linac and Booster, while leaving the Storage Ring unaffected.

Time adjustment offers:

• in theory, "fixed" step size, without analog ambiguities and drift.

Taking the "Time Adjustment" (fixed RF phase) case, the extreme example would be where the two rings have N and N+1 buckets. By waiting long enough, any two buckets would be aligned. Since the SLS design does not use a Resonant Power Supply for the Booster, it is possible to wait an arbitrary period, even as large as hundreds of microseconds.

In SLS, 450 RF buckets are used for the Booster and 480 for the storage ring. Given this, Bucket #0 in the Booster increments its alignment with Bucket #0 of the Storage Ring in multiples of 30. Thus, the incrementing of Minor Steps less than 30 must be implemented

with high-speed counter or phase-shifter, while the multiples of 30 can be done simply by waiting for another booster rotation period. The Minor Steps are used to send the gun trigger to the linac, since this is the only element of the machine which can respond in less than an RF period.

3.5.8 Bunch Clock

The Bunch Clock is being developed early in the project, so a simple manual control of the RF bucket number, the burst length and a single shot cycle is required for testing; this manual control would be designed to mate into a standard VME card when the control hardware and software is available. The front view in Fig.f358_a shows a very straight-forward user interface. A further substantial simplification is achieved by including (for no extra cost) presettable precision delays into each of the pulsed power supplies. Thus the single fibre optic data output from the bunch clock is split and sent directly to the Machine Timing Receivers in the VMEs. By using modern LSI technology, there are less than 30 integrated circuits in this unit, and much of the space inside is for cooling.



Fig.f358 a: Front view of the manual control panel for the Bunch Clock



Rear View

Fig.f358 b: Rear panel of the Bunch Clock

The rear panel in Fig.f358_b shows the phase-critical signals presented on N-type connectors in the upper section, while the single fibre optic output (with timing pulses for monitoring only) in the lower section.



Fig.f358 c: Simplified circuit of the Bunch Clock

Fig. f358_c shows the outline of the bunch clock. The largest common divisor of 450 and 480 is 30. This fixes the word rate for the Machine Timing at 30/500MHz = 60nsec. The option for phase shifting the Booster and Linac RF with a vector modulator is included. This can be achieved with very coarse increments using GaAs switches and miniature delay lines; the only requirement is that after a shift of 2π , the phase returns to the original value. Increments in the Superperiod occur when both the Storage Ring and Booster buckets return to their original alignment. This occurs every 15.36µsec, which presents no speed difficulty for the string of divide-by-N counters that generate the required machine timing pulses. The divide-by-N counters start counting Superperiods when the "Fire" command is given, and stop when they reach their programmed count value.

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